Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A solution-processed thin film transistor formation method, comprising steps of:

forming conductive solution-processed thin film contacts, semiconductor solution-processed thin film active regions, and dielectric solution-processed thin film isolations in a sequence and organization to form a solution-processed thin film structure capable of transistor operation; and

selectively ablating one or more of the semiconductor solution-processed thin film active regions and the dielectric solution-processed thin film isolations to pattern or complete patterning of a material being selectively ablated, wherein said step of selectively ablating is carried out during or after said step of forming.

2. (Original) The method of claim 1, wherein said step of selectively ablating is applied to complete patterning of a material roughly patterned when deposited.

3. (Original) The method of claim 2, wherein the material roughly patterned when deposited is patterned as a result of a inkjet deposition process.

4. (Original) The method of claim 2, wherein the material roughly patterned when deposited is patterned as a result of a spin coat deposition process.

5. (Original) The method of claim 1, repeated to form a plurality of thin film structures capable of transistor operation and further comprising a step of forming device isolations by ablating material between structures.

6. (Original) The method of claim 5, further comprising a step of filing the device isolations with dielectric solution-processed thin film material.

7. (Original) The method of claim 5, wherein the conductive solution-processed thin film contacts are patterned to form a circuit interconnect pattern.

8. (Original) The method of claim 1, wherein said steps of forming and ablating comprise the following steps:

depositing drain and source conductive solution-processed thin film material upon a substrate;

selectively ablating a transistor channel in the drain and source conductive solution-processed thin films to form drain and source contacts;

depositing active region semiconductor solution-processed thin film material over the drain and source contacts and the substrate;

depositing isolation region dielectric solution-processed thin film material over the semiconductor solution-processed thin film material; and

depositing gate conductive solution-processed thin film material upon the isolation region dielectric to form a gate contact.

9. (Original) The method of claim 8, wherein said steps of depositing drain and source conductive solution-processed thin film material and depositing gate conductive material solution-processed thin film material comprise inkjet printing conductive solution-processed thin film material.

10. (Original) The method of claim 9, wherein:

said step of depositing active region semiconductor solution-processed thin film material comprises spin coating dielectric solution-processed thin film material; and

said step of depositing isolation region dielectric solution-processed thin film material comprise spin coating dielectric solution-processed thin film material.

11. (Original) The method of claim 8, wherein the transistor channel is formed to be 5μm or less wide.

12. (Original) The method of claim 1, wherein said steps of forming and ablating comprise the following steps:

depositing gate conductive solution-processed thin film material upon a substrate;

depositing isolation region dielectric solution-processed thin film material over the gate conductive solution-processed thin film material and the substrate;

depositing active region semiconductor solution-processed thin film material over the isolation region dielectric; and

depositing drain and source conductive solution-processed thin film material upon the active region semiconductor solution-processed thin film material; and

selectively ablating a transistor channel in the drain and source conductive solution-processed thin film material to form drain and source contacts.

13. (Original) The method of claim 12, wherein said steps of depositing drain and source conductive solution-processed thin film and depositing gate conductive solution-processed thin film materials comprise inkjet printing conductive solution-processed thin film material.

14. (Original) The method of claim 13, wherein:

said step of depositing active region semiconductor solution-processed thin film material comprises spin coating semiconductor solution-processed thin film material and

said step of depositing isolation region dielectric solution-processed thin film material comprises spin coating dielectric solution-processed thin film material.

15. (Original) The method of claim 1, wherein said steps of forming and ablating comprise the following steps:

depositing gate conductive solution-processed thin film material upon a substrate;

depositing isolation region dielectric solution-processed thin film material over the gate conductive solution-processed thin film material and the substrate;

depositing drain and source conductive solution-processed thin film material upon the isolation region dielectric solution-processed thin film material;

selectively ablating a transistor channel in the drain and source conductive solution-processed thin film material to form drain and source contacts;

depositing active region semiconductor solution-processed thin film material over the drain and source conductive solution-processed thin film material and the isolation dielectric.

16. (Previously Presented) The method of claim 15, wherein said steps of depositing source and drain conductive solution-processed thin films and depositing gate conductive solution-processed thin film material comprise inkjet printing conductive solution-processed thin film material.

17. (Original) The method of claim 16, wherein;

said step of depositing active region semiconductor solution-processed thin film material comprises spin coating semiconductor solution-processed thin film material; and

said step of depositing isolation region dielectric solution-processed thin film material comprising spin coating dielectric solution-processed thin film material.

18. (Original) The method of claim 1, wherein said step of selectively ablating uses a laser wavelength tuned to be absorbed by material being ablated and to minimally damage material underlying material being ablated.

19. (Original) The method of claim 1, wherein said step of selectively ablating is conducted through an optical mask to ablate multiple features simultaneously.

20. (Original) The method of claim 1, wherein said step of selectively ablating is carried out while varying one or both of a laser wavelength and intensity.

21. (Currently Amended) A solution-processed thin film transistor formation method, comprising steps of:

forming solution-processed thin film layers into a transistor structure, wherein the transistor structure includes a semiconductor solution-processed thin film active region, and a dielectric solution-processed thin film isolation; and

during said forming, patterning the semiconductor solution-processed thin film active region and the dielectric solution-processed thin film isolation ~~portions of the transistor structure~~ via laser ablation, using laser wavelength tuned to be absorbed by material being patterned and to minimally damage material underlying material being patterned.

22. (Original) The method of claim 21, wherein said step of patterning is applied to complete patterning of a material roughly patterned when deposited.

23. (Original) The method of claim 22, wherein the material roughly patterned when deposited is patterned as a result of an inkjet deposition process.

24. (Original) The method of claim 22, wherein the material roughly patterned when deposited is patterned as a result of a spin coat deposition process.

25. (Original) The method of claim 21, repeated to form a plurality of thin film structures capable of transistor operation and further comprising a step of forming device isolations by ablating material between structures.

26. (Original) The method of claim 25, further comprising a step of filling said device isolations with dielectric solution-processed thin film material.

27. (Original) The method of claim 21, wherein said step of patterning is conducted through an optical mask to ablate multiple features simultaneously.

28. (Original) The method of claim 21, wherein said step of patterning is carried out while varying one or both of a laser wavelength and intensity.

29. (Currently Amended) A solution-processed thin film transistor including drain, source and gate contacts formed of conductive solution-processed thin film materials, a semiconductor solution-processed thin film material active region contacting the drain and source contacts and isolated from the gate contact by a dielectric solution-processed thin film material, the transistor being formed by a process comprising steps of:

depositing, in a ~~rough~~ pattern, the drain and source contacts, and

selectively ablating the semiconductor solution-processed thin film active region ~~refining the rough pattern by selective laser ablation of the drain and source contacts~~.

30. (Original) The method of claim 29, wherein said step of refining creates a transistor channel.

31. (Original) The method of claim 29, wherein said step of refining is conducted through an optical mask to ablate multiple features simultaneously.

32. (Original) The method of claim 29, wherein said step of refining is carried out while varying one or both of a laser wavelength and intensity.

33. (Previously Presented) The method of claim 1, wherein selectively ablating includes a conductive solution-processed thin film contact.

34. (Previously Presented) The method of claim 21, wherein the transistor structure includes a solution-processed thin film contact.

35. (New) A solution-processed thin film transistor formation method, comprising steps of:

forming solution-processed thin film layers into a transistor structure, wherein the transistor structure includes a semiconductor solution-processed thin film active region, and a dielectric solution-processed thin film isolation;

during said forming, patterning portions of the transistor structure via laser ablation, using laser wavelength tuned to be absorbed by material being patterned and to minimally damage material underlying material being patterned; and

repeating the forming and patterning to form a plurality of thin film structures capable of transistor operation and further comprising a step of forming device isolations by ablating material between structures.

36. (New) The method of claim 35, further comprising a step of filling said device isolations with dielectric solution-processed thin film material.